

IN THE UNITED STATES PATENT AND TRADEMARK OFFICE

In re Application of:)
)
Koji USUDA et al.)
) Group Art Unit:
Serial No.: Not Yet Assigned)
) Examiner:
Filed: July 28, 2003)
)
For: SEMICONDUCTOR)
APPARATUS)

**Commissioner for Patents
P.O. Box 1450
Alexandria, VA 22313-1450**

Sir:

INFORMATION DISCLOSURE STATEMENT UNDER 37 C.F.R. § 1.97(b)

Pursuant to 37 C.F.R. §§1.56 and 1.97(b), applicants bring to the Examiner's attention the documents listed on attached Form PTO-1449. Copies of the listed documents are attached. Applicants respectfully request that the Examiner consider the documents listed on attached Form PTO-1449 and indicate that they were considered by making an appropriate notation on this form.

This Information Disclosure Statement is being filed with the above-referenced application.

This submission does not represent that a search has been made or that no better art exists and does not constitute an admission that each or all of the listed documents are material or constitute "prior art." If the Examiner applies any of the documents as prior art against any claim in the application and applicants determine that the cited documents do not constitute "prior art" under United States law, applicants

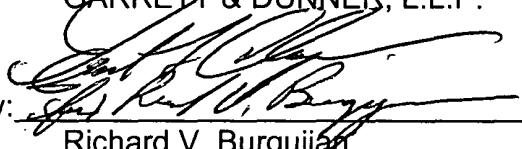
reserve the right to present to the office the relevant facts and law regarding the appropriate status of such documents. Applicants further reserve the right to take appropriate action to establish the patentability of the disclosed invention over the listed documents, should one or more of the documents be applied against the claims of the present application.

If there is any fee due in connection with the filing of this Statement, please charge the fee to our Deposit Account No. 06-0916.

Respectfully submitted,

FINNEGAN, HENDERSON, FARABOW,
GARRETT & DUNNER, L.L.P.

Dated: July 28, 2003

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Enclosures
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INFORMATION DISCLOSURE CITATION

Atty. Docket No.	04329.3101	Serial No.	
Applicant	Koji USUDA et al.		
Filing Date	July 28, 2003	Group:	

U.S. PATENT DOCUMENTS							
Examiner Initial*		Document Number	Issue Date	Name	Class	Sub Class	Filing Date If Appropriate

FOREIGN PATENT DOCUMENTS							
		Document Number	Publication Date	Country	Class	Sub Class	Translation Yes or No

OTHER DOCUMENTS (Including Author, Title, Date, Pertinent Pages, Etc.)	
	McKee et al. "PHYSICAL STRUCTURE AND INVERSION CHARGE AT A SEMICONDUCTOR INTERFACE WITH A CRYSTALLINE OXIDE", Science, Vol. 293, pages 468-471, (2001)
	Nishikawa et al., "DIRECT GROWTH OF SINGLE CRYSTALLINE CeO ₂ HIGH-K GATE DIELECTRICS", Extended Abstracts of the 2001 International Conference on Solid State Devices and Materials, pages 174-175, (2001)
	Gottschalk et al., "EPITAXIAL Pr ₂ O ₃ ON SILICON AS AN ALTERNATIVE GATE OXIDE FOR FUTURE CMOS APPLICATIONS", JOINT SESSION CRYSTALLINE OXIDES FOR GATE DIELECTRICS, Session N8.5/T6.5, pages 350-351, (2002)
	Tezuka et al., "NOVEL FULLY-DEPLETED SiGe-ON-INSULATOR pMOSFETs WITH HIGH-MOBILITY SiGe SURFACE CHANNELS", IEDM Tech. Dig., 946, IEEE, (2001)
	Welser et al.; "STRAIN DEPENDENCE OF THE PERFORMANCE ENHANCEMENT IN STRAINED-Si <i>n</i> -MOSFETs"; IEDM, pages, 373-376, IEEE, (1994)
	Hirose et al.; "FUNDAMENTAL LIMIT OF GATE OXIDE THICKNESS SCALING IN ADVANCED MOSFETs"; Semicond. Sci. Technol. Vol. 15, pages 485-490, (2000)

Examiner	Date Considered
*Examiner: Initial if reference considered, whether or not citation is in conformance with MPEP 609; draw line through citation if not in conformance and not considered. Include copy of this form with next communication to applicant.	
Form PTO 1449	Patent and Trademark Office - U.S. Department of Commerce